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COUPLING OF SIGNALS BETWEEN ADJACENT FUNCTIONAL BLOCKS IN AN INTEGRATED CIRCUIT CHIP

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Prov. App. Nos. 60/477,338 filed June 11, 2003, and 60/488,800 filed July 22, 2003, each entitled "MEMORY CELL FOR MODIFICATION OF REVISION IDENTIFIER AND/OR DEFAULT REGISTER VALUES IN AN INTEGRATED CIRCUIT CHIP AND METHOD FOR MANUFACTURING SAME," and which are incorporated by reference herein in their entirety.

[0002] This application is related to U.S. App. No. 10/697,079, entitled "MEMORY CELL FOR MODIFICATION OF REVISION IDENTIFIER IN AN INTEGRATED CIRCUIT CHIP" (Atty. Doc. No. 1875.4360002); U.S App. No. 10/697,889, entitled "METHOD FOR MANUFACTURING A MEMORY CELL FOR MODIFICATION OF REVISION IDENTIFIER IN AN INTEGRATED CIRCUIT CHIP" (Atty. Doc. No. 1875.4360003); and U.S App. No. 10/697,286, entitled "MEMORY CELL FOR MODIFICATION OF DEFAULT REGISTER VALUES IN AN INTEGRATED CIRCUIT CHIP" (Atty. Doc. No. 1875.4360004), all filed concurrently herewith, which are all incorporated by reference herein in their entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0003] The present invention is directed to integrated circuit (IC) chips, and more particularly to coupling of power, control and data signals between adjacent functional blocks in an IC.